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Breakdown Enhancement in Silicon Nanowire *p-n* Junctions

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ABSTRACT

We demonstrate highly reproducible silicon nanowire diodes fabricated with a fully VLSI compatible etching technology, with diameters down to 30 nm. A contact technology based on recrystallized polysilicon enables specific contact resistances as low as $\rho \approx 10^{-7}$ Ω cm². Our devices show a strongly diameter-dependent breakdown voltage at reverse bias, which we explain in terms of the influence of the surrounding dielectric. We suggest that this technology is suitable for incorporating nanowire-based functionalities into future integrated circuits.

Semiconducting nanowires are widely being investigated as components for future integrated circuits. A variety of electronic devices have been realized using nanowires, ranging from field-effect transistors[1] and photodiodes[2] to biosensors[3] and neural stimulation devices.[4] These devices are typically based on the field-effect, made from grown wires using a gold catalyst, and feature metal−semiconductor junctions for the supply and extraction of carriers. Although their performance and breadth of applications is impressive, these devices cannot easily be integrated into modern VLSI processes.

In this work, we investigate silicon nanowire *p-n* junctions, made using a fully VLSI compatible, "top-down" etching technology. Such devices represent the most basic nanowire device component and have not been systematically investigated in silicon. One reason for this lack of results on basic nanowire *p-n* junctions lies in the difficulty of manufacturing high quality devices. On the one hand, controlled doping and contacting of nanowires is difficult in practice;[5] in addition, random dopant fluctuations are expected to dominate the device behavior at small wire diameters. On the other hand, unwanted leakage currents at the perimeter of a *p-n* junction are a notorious nuisance in the device fabrication of any *p-n* junction and can be expected to completely dominate the currents in a nanowire diode. These practical problems aside, an important question in nanoscale device physics concerns the limits of conventional drift-diffusion models for electrons and holes. The concepts of minority concentration gradients, continuum distributions of dopants and traps appear increasingly implausible when one considers the small semiconductor volume inside nanowire devices.

Furthermore, as device dimensions shrink, the potential landscape inside the semiconductor becomes increasingly influenced by the surrounding material. For the case of junctions embedded in SiO_2, dielectric field shaping has been known for some time to enhance breakdown voltages of planar diodes.[6] We show here that these effects are very pronounced in nanowires.

To experimentally study nanowire diodes, we have used state-of-the-art silicon VLSI techniques to realize *p-n* junctions on a silicon wafer. We started with arsenic doped wafers (8″ Electronic Grade Si, ⟨100⟩ Czochralski, $\rho \approx 3$ mΩ cm or $N_{As} \approx 2 \times 10^{19}$ cm^{-3}, 500 nm lowly doped epitaxial layer; from Wacker Siltronic). Into these wafers, we implanted boron ions to form a highly doped anode and annealed out the implant damage (0.5 keV, 10^{15} atoms/cm², 1100 °C spike anneal, 0 s soak time). We then used a Halogen-based inductively coupled plasma-etch to form the nanowires (see Supporting Information). An anneal in hydrogen ambient (900 °C, 2 min, 760 torr, ASM Epsilon) is used as a surface treatment of the etched nanowires, to remove any etch damage and reshape the nanowire.[7] The etched and annealed wires were embedded in SiO_2 using a combination of densified tetraethoxysilane (TEOS) and high-density plasma assisted oxide. Chemical-mechanical polishing was used to planarize the structures. After exposing the nanowire tips by using 2% HF acid, the tips are cleaned and rendered hydrophobic (Ozone gas, diluted HF, Marangoni dry). To contact the silicon nanowires, we used chemical vapor deposition to deposit ∼150 nm of in-situ boron-doped polysilicon (typically $\rho < 1$ mΩ cm), with minimal interfacial oxide formation. This highly doped polysilicon contact layer avoids any metal-nanowire contacts in our system, and indeed any Schottky barrier contacts. After pattering of contact pads (200 μm × 200 μm), the top of the polysilicon film was converted to NiSi using sputtered Ni, annealed at 450 °C. Both these contact pads and the back-side of the wafer were further metallized with evaporated aluminum.

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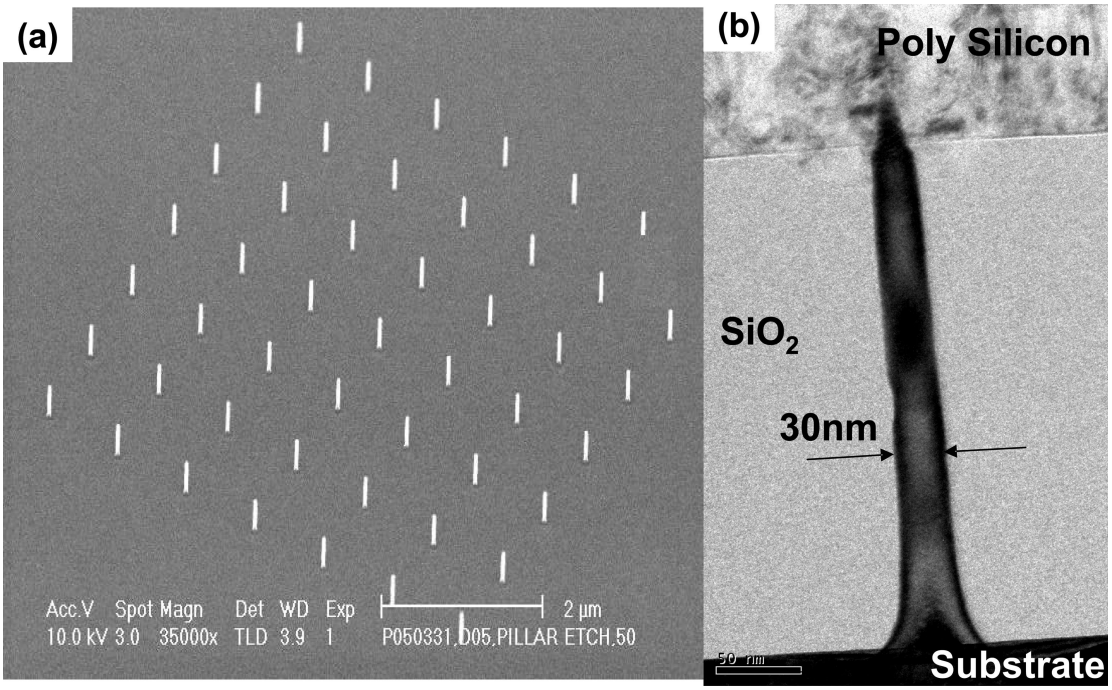

Figure 1. (a) A scanning electron micrograph of an array of 50 silicon nanowires, after plasma etching; (b) a transmission electron micrograph of a single 30 nm silicon nanowire. At the tip of the nanowire, the polysilicon contact layer has recrystallized to form a low-resistance ohmic contact.

Transmission electron micrographs (Figure 1) show that our smallest devices have a uniform diameter of ~30 nm (aspect ratio ≈ 1:10), with negligible tapering, and no morphological trace of residual implant damage. From our analysis of the manufacturing process we estimate the junction depth to be about 100 nm below the top end (anode) of the nanowires (see Supporting Information). Our electron micrograph also indicates that the polysilicon contact layer has recrystallized around the tip of the nanowire during one of the thermal anneal steps in the process. This indicates an intimate contact between the nanowire and the polycrystalline contact layer. With this contact technology we expect to avoid any uncertainties owing to nanoscale Schottky barriers.

In Figure 2a we show the forward bias current−voltage characteristics of an array of 50 nanowire diodes, each ~30 nm wide. Our devices show diode characteristics over 11 decades in current with a maximum current density of about 1600 kA/cm^2 per wire, assuming uniform current flow over the whole wire diameter. The absence of a bias-independent leakage current indicates that the surface has been effectively passivated. These characteristics are highly reproducible, and the forward bias current is proportional to the number of wires per bond-pad (see inset, Figure 2a). A study of 29 different sites on our wafer shows a spread of about 20% in the forward current. Figure 2b shows the product of the current I and the differential resistance $r_j = dV/dI$ at high currents, for one individual 30 nm diode. According to standard diode theory,[8] $r_jI = nv_{th} + R_{ser}I$, where n is the diode ideality factor, v_{th} is the thermal voltage and R_{ser} is the diode series resistance. For the typical diode shown in Figure 2b, we extract a diode series resistance of $R_{ser} \approx 9.2$ kΩ and an ideality factor of $n = 2.0$. Depending on the actual contact area in this particular device, we estimate the

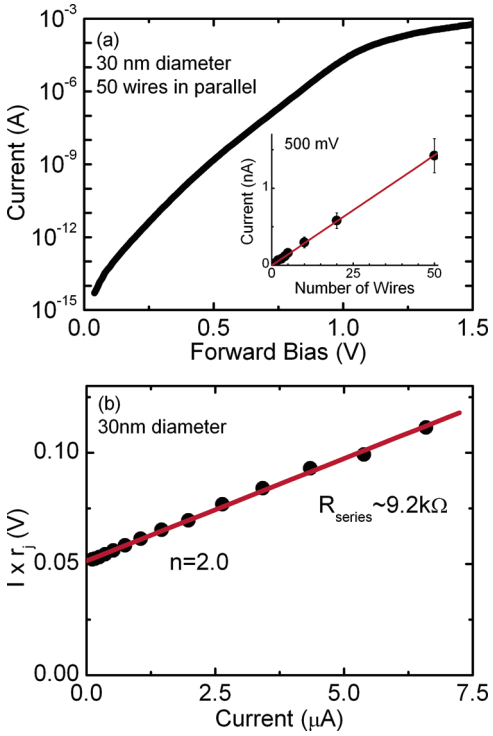

Figure 2. (a) The forward bias diode characteristics of an array of 50 nanowire diodes, each ~30 nm diameter. The inset shows the scaling plot of forward bias current vs number of nanowires per contact. Error bars are ±1 σ from a sample of 29 dies. (b) The ideality factor and series resistance for one individual diode, extracted at high forward currents.

specific contact resistance to be in the range of 6−20 Ω μm^2, consistent with published values on the polysilicon contact resistance in state-of-the-art bipolar transistors.[9] The diode ideality factor is similar to what was found recently in

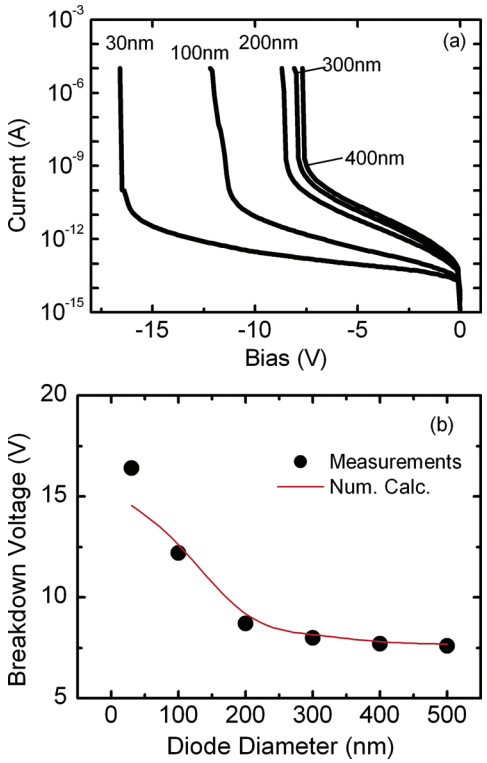

Figure 3. (a) The reverse bias diode characteristics for devices of various diameters; (b) the measured (dots) and calculated (lines) breakdown voltages as a function of nanowire diameter.

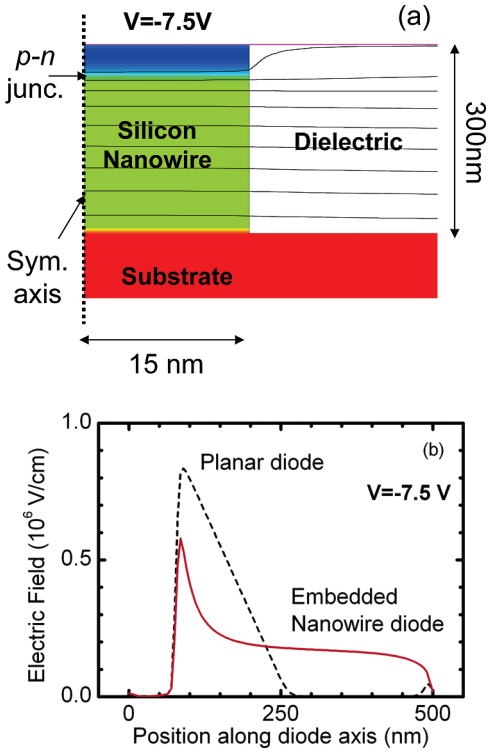

Figure 4. (a) The calculated electrostatic equipotential lines in the vicinity of the nanowire (spacing = 1 V); (b) the calculated electric field profile along the symmetry axis of the wire (solid line) and the equivalent field profile for a planar diode (dashed line) at a reverse bias of −7.5 V.

Germanium nanowire diodes[5] with a diameter of 40 nm. Future research will examine the origin of the nonideal diode current in more detail.

We next turn to the behavior at reverse bias, where we observe significant differences for different diode diameters, shown in Figure 3. For our structures which are ∼500 nm in diameter, the breakdown voltage is around 7.6 V. As the lateral dimension of the diode is reduced to 30 nm, the breakdown voltage is increased by more than a factor of 2 to 16.9 V. In Figure 3b, we show the diameter dependence of the breakdown voltage, along with numerical calculations.[10]

We ascribe this breakdown enhancement primarily to the influence of the surrounding dielectric on the electric field profile in the silicon nanowire *p-n* junction itself, a phenomenon well-known in planar power devices.[6,11] In essence, the anode contact defined by the polysilicon contact layer and the highly doped substrate form two large capacitor plates. The medium between these capacitor plates is almost entirely SiO_2 dielectric, and the 30 nm silicon nanowires make up less than 1% of the area. The field distribution away from the silicon nanowires is thus uniform, with the equally spaced equipotential planes typical of a simple capacitor. At the boundary between the embedding dielectric and the silicon nanowires, the continuity requirements of the electrostatic field and displacement smooth out the electric field profile inside the junction and suppress the field peak responsible for the avalanche breakdown of the diode.

This effect can be modeled with numerical solutions to Poisson's equation in the semiconductor and dielectric using the appropriate boundary conditions (See Supporting Information), and the results are shown as the line in Figure 3b and in Figure 4. For our calculations, we assumed a one-sided junction with a uniform donor concentration of $\sim 3 \times 10^{17}\text{cm}^{-3}$, which is in agreement with the breakdown voltage for the 500 nm diodes. Apart from this parameter, we make no other adjustments and calculate the solutions to Poisson's equation in cylindrical co-ordinates for various diode diameters. The breakdown voltage is then calculated from the impact ionization integral following standard formulations.[8]

Figure 4a shows equipotential lines in the vicinity of the nanowire diode at a reverse bias close to the breakdown voltage of the equivalent planar diode. It shows how the electrostatic potential changes from the uniform distribution of the dielectric to the field profile inside the semiconductor junction. Inside the dielectric, the width over which the electric field deviates strongly from the uniform field is of the order of 35 nm. This indicates that the breakdown enhancement effect seen here should persist for very densely packed nanowire diodes.

A comparison between the electric field in the nanowire diode and the conventional planar diode is shown in Figure 4b. The smearing out of the field distribution and the resulting reduction in the electric field peak near the metallurgical junction is clearly seen.

Although our simple model can reproduce the breakdown enhancement well, as shown in Figure 3b, it cannot give complete quantitative agreement with our measurements at

the smallest diameter. This may well be due to effects not included in our model, such as strain in the semiconductor, fixed charges in the dielectric, short-comings of the standard avalanche model, or indeed uncertainties in the doping profiles of the devices. Quantum effects such as band gap widening, modified phonon scattering rates, or effects due to a 1D density-of-states can also be expected to modify breakdown voltages in a nanowire. However, these effects are thought to appear at smaller nanowire diameters in silicon.[12] Unambiguous identification of these quantum effects on device behavior will require similarly controlled and reproducible nanowire technologies, at smaller diameters than those we present here.

In summary, we have demonstrated embedded silicon nanowire *p-n* junction diodes, with diameters down to 30 nm. Our diodes show an enhancement in their breakdown voltages by a factor of ~2 over their planar equivalent. The potential landscape that charge carriers experience in these devices is controlled by the surrounding dielectric, which smears out of the electric field inside the semiconductor junction. This in turn results in the suppression of avalanche breakdown.

We have also demonstrated that state-of-the-art "top down" manufacturing techniques are capable of producing highly reproducible nanowire junction devices, without any problems of placement or integration of wires, or indeed of contamination due to metallic precursors. A contact technology based on recrystallized polysilicon is also shown. This technique can be extended to even smaller nanowire diameters, and we suggest that it is suitable for the realization of a large range of junction based devices, as well as for an experimental test bed for quantum effects in even smaller nanowire devices.

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Supporting Information Available: Nanowire etching, junction depth estimate, and numerical simulations. This material is available free of charge via the Internet at http://pubs.acs.org.

References

(1) Goldberger, J.; Hochbaum, A. I.; Fan, R.; Yang, P. *Nano Lett.* **2006**, *6* (5), 973−977.
(2) Hayden, O.; Agarwal, R.; Lieber, C. *Nat. Mater.* **2006**, *5* (5), 352−356.
(3) Yi, C.; Qingqiao, W.; Hongkun, P.; Lieber, C. *Science* **2001**, *293* (5533), 1289−1292.
(4) Patolsky, F.; Timko, B.; Yu, G.; Fang, Y.; Greytak, A.; Zheng, G.; Lieber, C. *Science* **2006**, *313* (5790), 1100−1104.
(5) Tutuc, E.; Appenzeller, J.; Reuter, M. C.; Guha, S. *Nano Lett.* **2006**, *6* (9), 2070−2074.
(6) Appels, J. A.; Vaes, H. M. J. *IEDM Tech. Dig.* **1979**, 238−241.
(7) Lee, M.; Wu, M. *J. Microelectromech. Syst.* **2006**, *15* (2), 338−343.
(8) Sze, S. M. *Physics of Semiconductor Devices*, 2nd ed.; Wiley: New York, 1981.
(9) Donkers, J. J. T. M.; Vanhoucke, T.; Agarwal, P.; Hueting, R. J. E.; Meunier-Beillard, P.; Vijayaraghavan, M. N.; Magnee, P. H. C.; Verheijen, M. A.; de Kort, R.; Slotboom, J. W. *IEDM Tech. Dig.* **2004**, 243−246.
(10) *Taurus-Medici*, version 2005.10; Synopsis Inc.: Mountain View, CA, 2007.
(11) Sonsky, J.; Heringa, A. *IEDM Tech. Dig.* **2005**, 4.
(12) Read, A.; Needs, R.; Nash, K.; Canham, L.; Calcott, P.; Qteish, A. *Phys. Rev. Lett.* **1992**, *69* (8), 1232−1235.

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